NB3H83905CDGEVB

NB3H83905CDGEVB Evaluation Board User's Manual

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EVAL BOARD USER'S MANUAL

Device Description

The NB3H83905CDG device is a 1.8 V, 2.5 V or 3.3 V VDD core Crystal input 1:6 LVTTL/LVCMOS fanout buffer with outputs powered by flexible 1.8 V, 2.5 V, or 3.3 V supply (with VDD ≥ VDDO). The core inputs accept a fundamental Parallel Resonant crystal from 3 MHz to 40 MHz or Single Ended LVCMOS Clock from 3 MHz to 100 MHz. Core supply must be equal or greater voltage than the output supply. See datasheet NB3H83905C/D (www.onsemi.com).

Evaluation Board Description

The NB3H83905CDGEVB Evaluation board is designed to provide a flexible and convenient platform to quickly program, evaluate and verify the performance and operation of the NB3H83905CDG SOIC−16 device under test. With the device removed, this NB3H83905CDGEVB Evaluation board is designed to accept a 16 Lead SOIC socket (M&M Specialties, Inc., 1−800−892−8760, www.mmspec.com, M&M #50−000−00112) to permit use as an insertion test fixture.

Board Features

- Crystal source mount, or external clock source (SMA) input. One 25 Mhz crystal is supplied.
- A SOIC−16 NB3H83905CDG device is solder mounted. The board may be adapted for insertion testing by removing the device and adding a 16 Lead SOIC socket (M&M #50−000−00112)
- Separate supply connectors for VDD, VDDO, SMAGND, and DUTGND (banana jacks and anvil clips)

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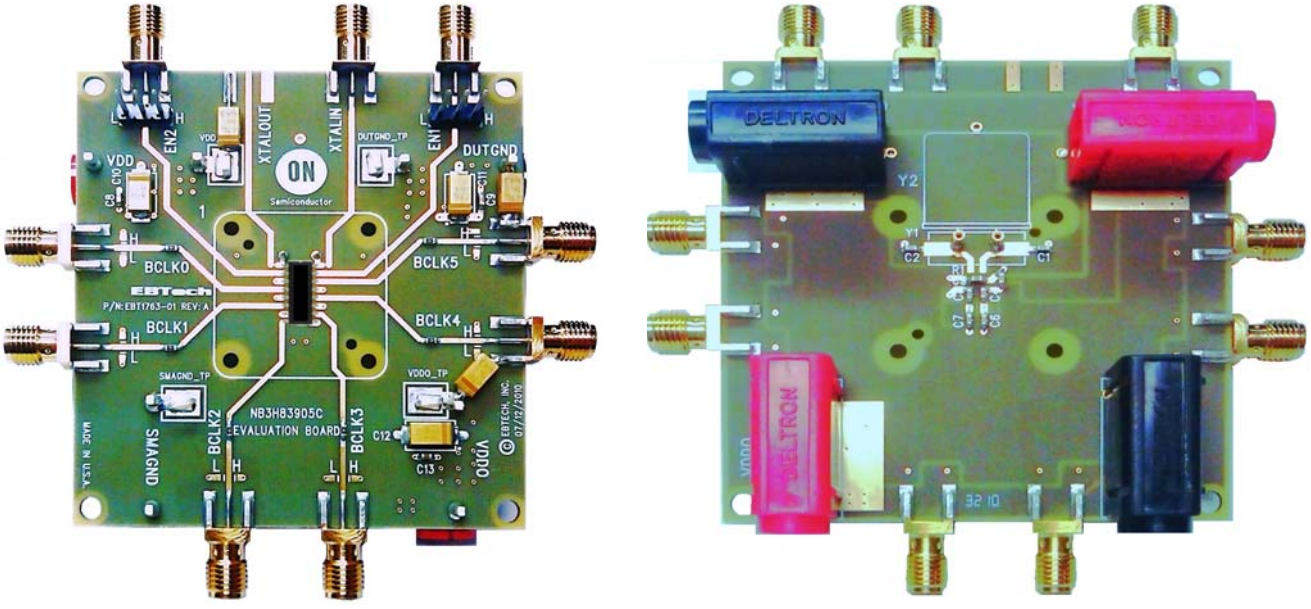

FRONT BACK

Figure 1. NB3H83905CDGEVB Evaluation Board

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Board Layout Maps

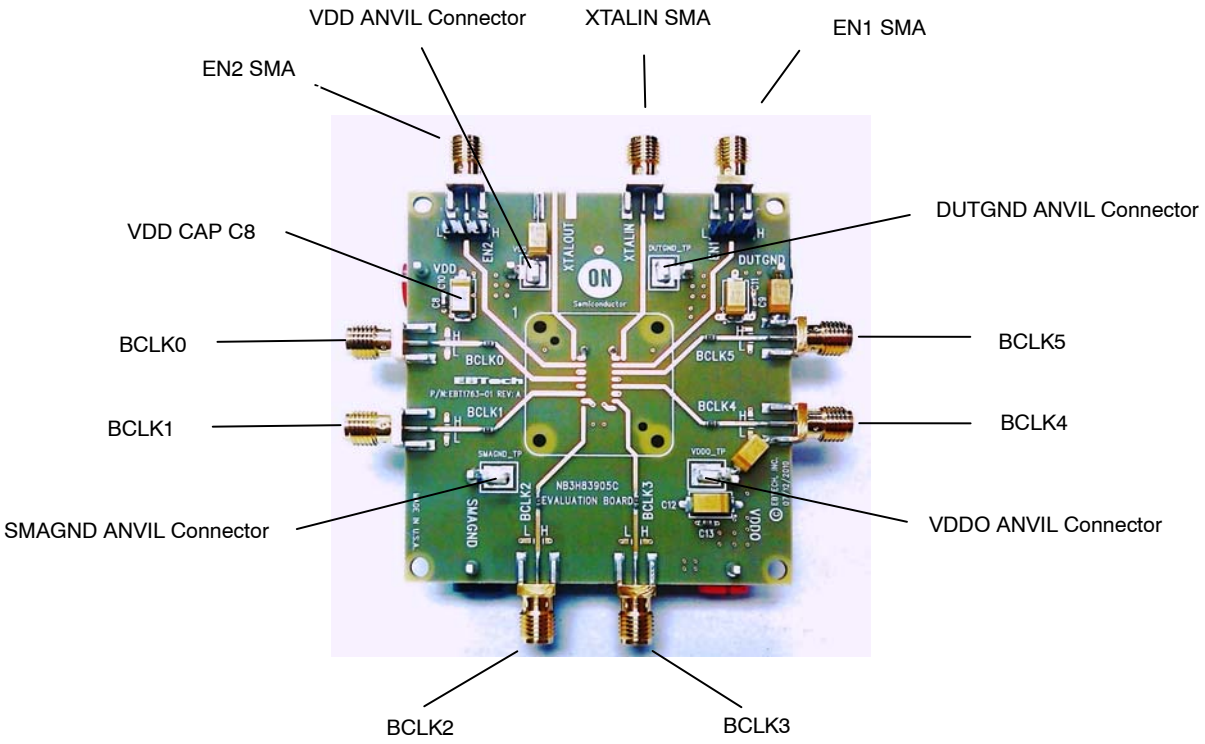


Figure 2. FRONT

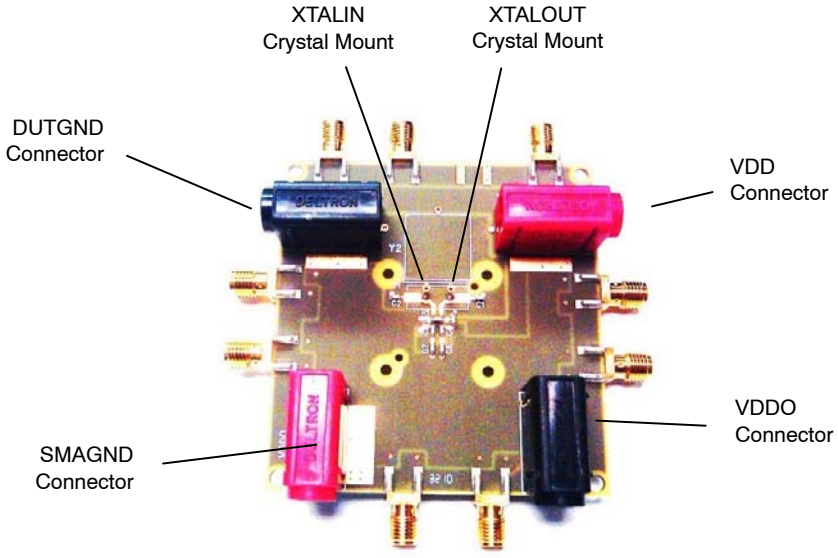


Figure 3. BACK

TEST AND MEASUREMENT SET−UP AND PROCEDURE

Step 1: Equipment

1.) Signal Generator: Agilent #33250A or HP8133 (or equivalent)

2.) Tektronix TDS8000 Oscilloscope

3.) Power Supply: Agilent #6624A or AG6626A DC (or equivalent)

4.) Digital Voltmeter: Agilent 34410A or 34401 (or equivalent)

5.) Matched Cables (> 20 GHz, SMA connectors): Storm or Semflex (or equivalent)

6.) Time Transition Convertor: Agilent 14534 250 ps (or equivalent)

7.) Phase noise Analyzer: Agilent E5052B (or equivalent)

Step 2: Lab Set−Up Procedure (Split Supplies into LOW impedance 50 Ohm equipment or probes)

1) **Test Supply Setup**: VDDO and GND Supplies may be centered on 0.0 V to permit direct connection to an Oscilloscope module (with 50 Ohm to GND) per Figure 4 and Table 1. Connect all board supplies using banana jack or clip anvil.

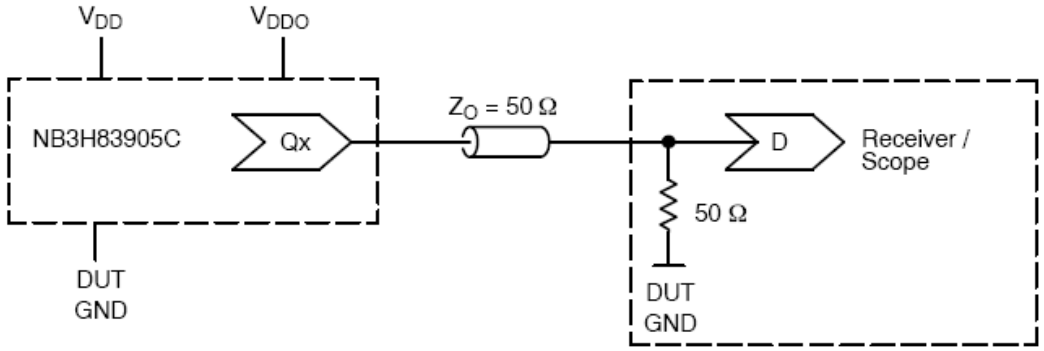


Figure 4. Typical Device Termination Setup and Termination Test Setup

Table 1. Test Voltages

Datasheet Spec Condition	TEST SETUP VDD	TEST SETUP VDDO	TEST SETUP DUT GND
VDD = VDDO = 3.135 V to 3.465 V (3.3 V Nom. ±5%)	1.56 to 1.73 V	1.56 to 1.73 V	−1.56 to −1.73 V
VDD = VDDO = 2.375 V to 2.625 V (2.5 V Nom. ±5%)	1.1875 to 1.3125 V	1.1875 to 1.3125 V	−1.1875 to −1.3125 V
VDD = VDDO = 1.6 V to 2.0 V (1.8 V Nom. ±0.2 V)	0.8 to 1.0 V	0.8 to 1.0 V	−0.8 to −1.0 V
VDD = 3.135 V to 3.465 V (3.3 V Nom.); VDDO =2.375 V to 2.625 V (2.5 V Nom.)	1.955 to 2.1525 V	1.1875 to 1.3125 V	−1.1875 to −1.3125 V
VDD=3.135 V to 3.465 V (3.3 V Nom.); VDDO=1.6 V to 2.0 V (1.8 V Nom.)	2.335 to 2.465 V	0.8 to 1.0 V	−0.8 to −1.0 V
VDD=2.375 V to 2.625 V (2.5 V Nom.); VDDO=1.6 V to 2.0 V (1.8 V Nom.)	1.575 to 1.625	0.8 to 1.0 V	−0.8 to −1.0 V

2.) **Inputs:**

For a Single Ended operation, bridge the small gap in located at the device footprint outline in the trace line to the SMA connector XTALIN. Use a LVCMOS Clock amplitude signal from 3 MHz to 100 MHz on the XTAL_IN/CLK pin16. Note the levels must be shifted according to the

supply voltages. Transitions Edges should about 250 ps or use TTC, Time transition Convertor, such as Agilent 14534 (250 ps) or an equivalent. Do not drive XTALOUT. Termination of the signal generator may be needed with 50 Ohms to SMA ground.

For Crystal operation use a fundamental Parallel Resonant crystal (see Datasheet Table 3) from 3 MHz to 40 MHz across pins 1 and 16. The Crystal mount is located on the back of the board and permanently connected to the device inputs by traces. Crystal Load capacitance (C1 and C2) values should consider all parasitic capacitances. Datasheet Figure 1 shows the typical NB3H83905C device crystal interface using a parallel resonant crystal. The frequency accuracy can be fine tuned by adjusting the C1 and C2 values. For example, a parallel crystal with loading capacitance C_L = 18 pF would use C1 = 15 pF and C2 = 15 pF as initial values. These values may be adjusted to fine tune frequency accuracy. Increasing the C1 and C2 values will reduce the operational frequency.

Enable 1 and 2 (see Datasheet Table 2) levels must be shifted according to the supply voltages. Open default condition will force a HIGH (enabled) due to an internal pullup resistor to VCC.

3.) **Outputs:**

Connect LVCMOS outputs to the oscilloscope with matched cables. NOTE: THE READINGS OF THE OUTPUT VOLTAGE LEVELS WILL BE OFFSET. With this split supply, the device outputs will be parallel terminated by the oscilloscope (or frequency counter) input module's internal 50 Ohms to GND impedance.

APPENDIX 1: DEVICE PIN TO BOARD CONNECTION INFORMATION (see current Datasheet)

Table 2. Device Pins to Board Connection

Device Pin	Board Connection	Name	I/O	Description
1		XTAL_OUT	Crystal Interface	Oscillator Output to drive Crystal
2		ENABLE 2	LVTTL / LVCMOS Input	Synchronous Enable Input for BCLK5 Output. Switches only when HIGH. Open default condition HIGH due to an internal pullup resistor to VCC.
3, 7, 11	DUTGND or DUTGND_TP	GND	GND	GND Supply pins. All VDD and VDDO pins must be externally connected to power supply to guarantee proper operation.
4, 6, 8, 10, 12, 14	BCLK0, 1, 2, 3, 4, 5	BCLK0, 1, 2, 3, 4, 5	LVCMOS Outputs	Buffered Clock outputs
5, 13	VDDO	VDDO	POWER	Output Positive Supply pins. All VDD and VDDO pins must be externally connected to power supply to guarantee proper operation. Bypass with 0.01 μF cap to GND.
9	VDD or VDD_TP	VDD	POWER	Output Positive Supply pins. All VDD and VDDO pins must be externally connected to power supply to guarantee proper operation. Bypass with 0.01 μF cap to GND.
15	EN1	ENABLE 1	LVTTL / LVCMOS Input	Synchronous Enable Input for BCLK0/1/2/3/4 Output block. Switches only when HIGH. Open default condition HIGH due to an internal pullup resistor to VCC
16	XTALIN	XTAL_IN/ CLK	Crystal Interface	Oscillator Input from Crystal. Single ended Clock Input.
	SMAGND or SMAGND_TP	SMAGND		SMA connectors GND. Should be connected equipment GND.

APPENDIX 2: BOARD TOP AND BOTTOM LAYER DESIGNS

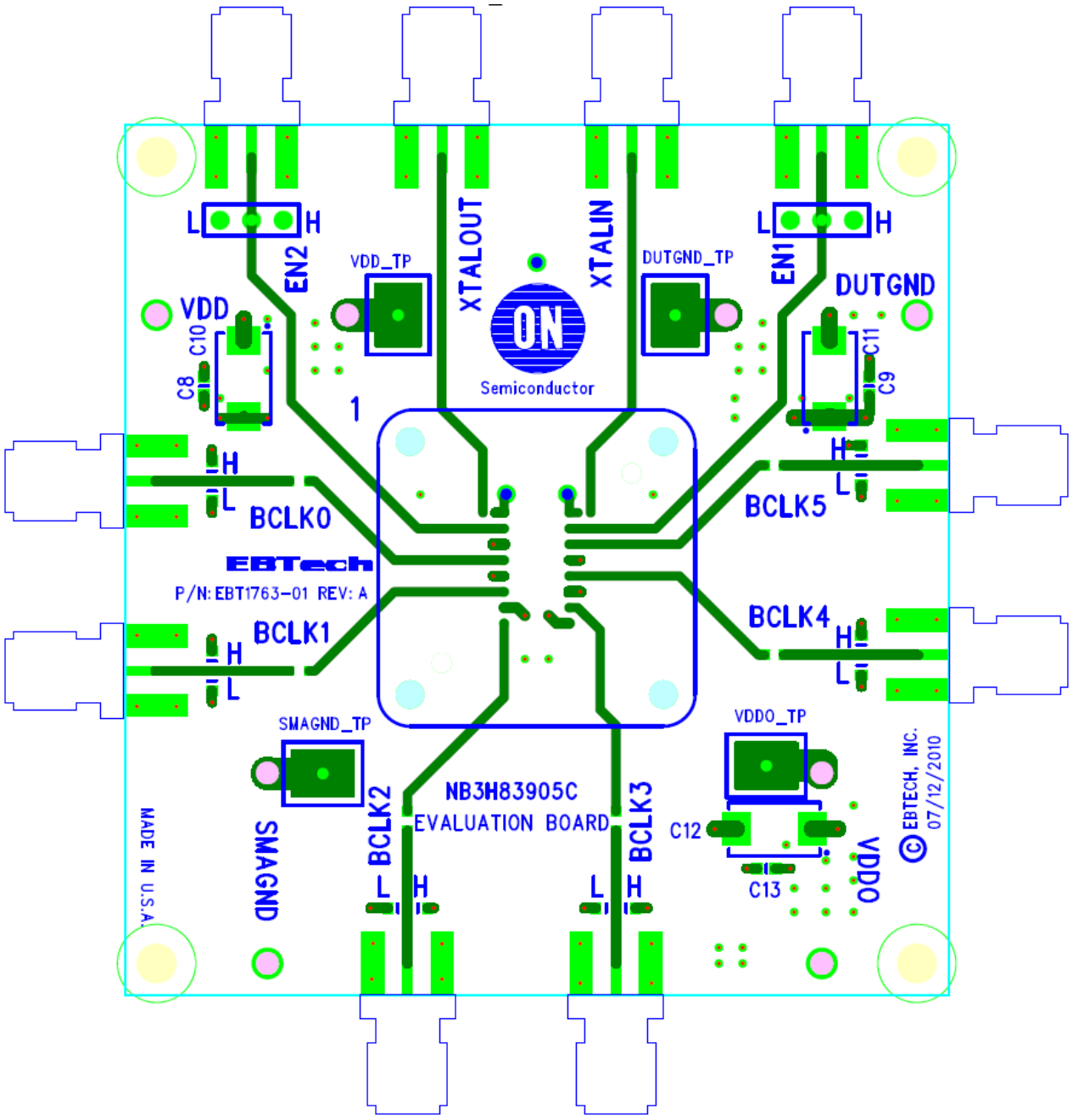


Figure 5. Top Layer Design

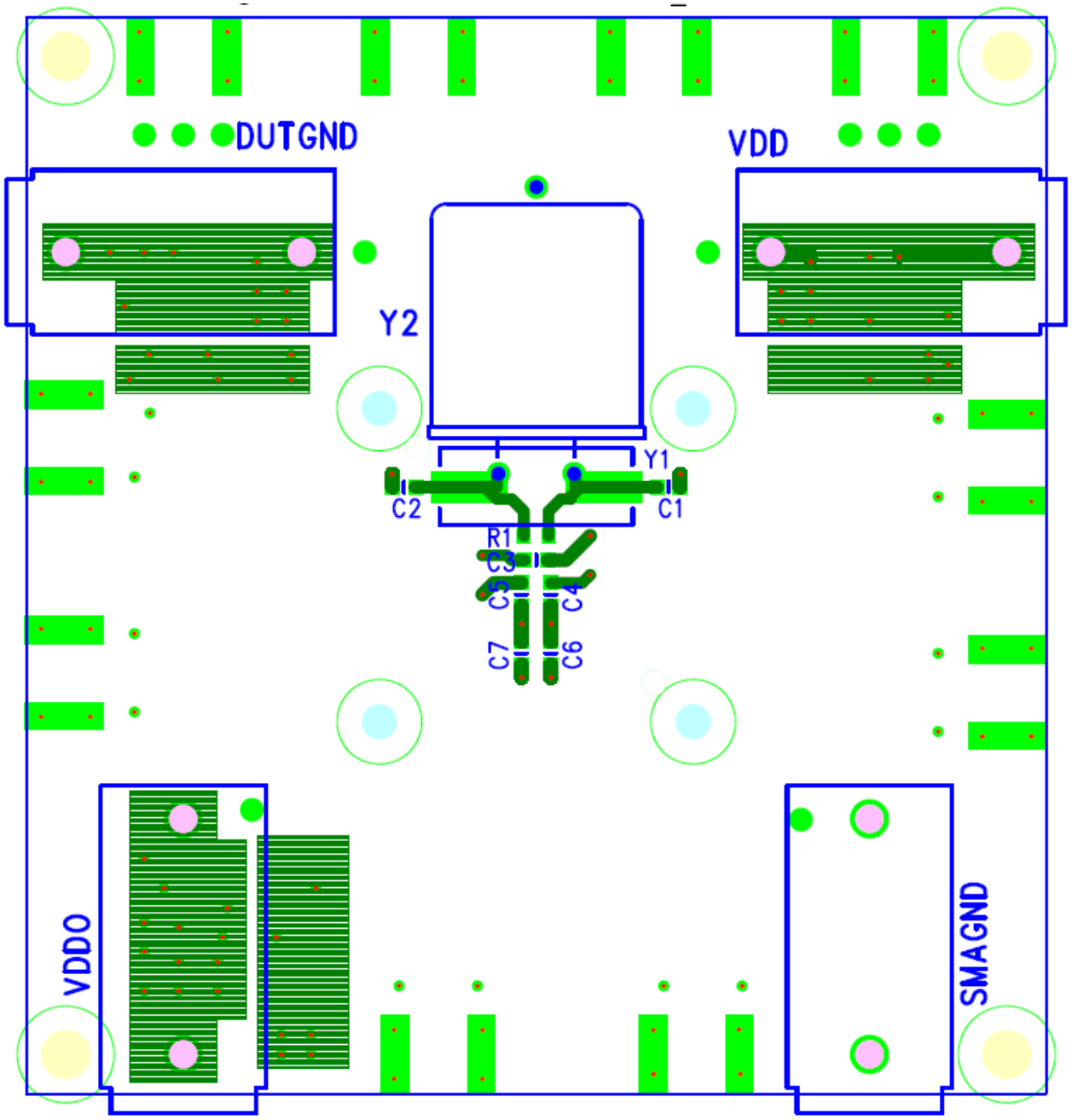
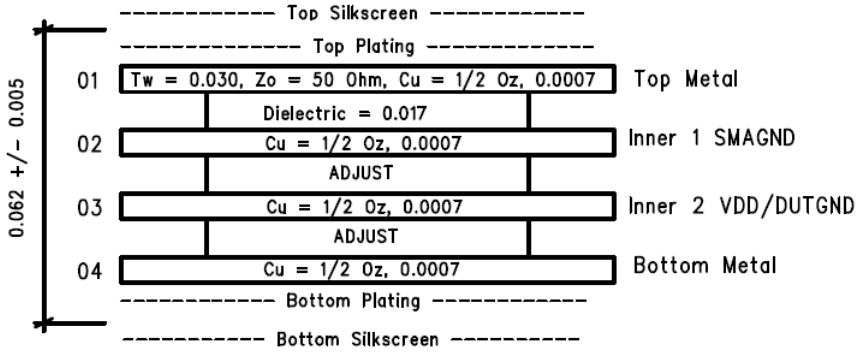


Figure 6. Bottom Layer Design

APPENDIX 3: BILL OF MATERIALS, LAMINATION STACKUP, AND ASSEMBLY NOTES

Components	Mfr / Part No.	Description	Supplier / Part Number	Qty
BANANA1 VDD, VDDO	Deltron / 579-0500	Connector, Banana Jack	Mouser / #164-6219	2
BANANA2 DUT GND, SMA GND	Deltron / 579-0500	Connector, Banana Jack, Deltron, Black #571-0500	Mouser / #164-6218	1
BANANA3 SMA GND	Deltron / 579-0500	Connector, Banana Jack, Deltron, Green #571-0500	Mouser / #164-7140	1
C4, C5, C6, C7, C8, C9	Kemet / C0805C104K5RACTU	Cap, Chip, 0.1 μF, 0805, 50V, 10%	Digi-Key / 399-1170-1-ND	6
C10, C11	Kemet / T491D226K016AS	Cap, Chip, 22 μF, 10%	Mouser / 80-T491D226K016AS	2
C1, C2	Kemet / C0805C150J1GACTU	Cap, Chip, 15 pF, 10%	Mouser / 80-C0805C150J1G	2
J1-J10	Johnson / #142-0711-821	PCB SMA Connector, SMA, Edge Mount	Mouser / 530-142-0711-821	2
JMP1, JMP2	SPC TECHNOLOGY / SPC20481	Header, Single Row, Pitch Spacing: 2.54 mm	Newark / 93K5734	2
Jumper Block Shunt	SPC TECHNOLOGY / SPC19808	Jumper, Pitch Spacing: 2.54 mm	Newark / 84K8570	2
SOCKET (OPT.)	M&M	SOIC-16 Direct Contact		(1)
XTAL	Abracon / ABL−25.000MHZ−B2F	25 Mhz Through Hole AT Cut Fundamental Crystal	Newark / 13J1637	1
XTAL Pin	Mill-Max	crystal pin receptacle / connector	#0462-0-15-15-11-27-04-0	2
Rx	Bourns / CR0603-J/-000ELF	Resistor, Chip, 0 Ω, 0603, 1/10 W, 1%	Mouser/652-CR0603-J/-000ELF	6

Lamination Stack



01 Top Metal
02 SMAGND
03 VDD / DUTGND
04 Bottom Metal

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